# Ebrahim Jahandar

## Personal Information's

*Full Name : Ebrahim Jahandar*
*Birthday : 15 June 1990*

## Contact Information's

*Emails : e {at} jahandar.ir*
*jahandar {at} ce.sharif.edu*
*Website : www.jahandar.ir*
*Postal Code : 48177-16389*

## Educations

**Ph.D @ Sharif University of Technology**
*2016 – Until Now - Computer Engineering*

**M.Sc @ Sharif University of Technology**
*2014- 2016 - Computer Architecture at Sharif CE*
*Design & Implementation of GPU Based Hardware Accelerator for DNS Servers*
*Under supervision of Dr Amir Hossein Jahangir*

**B.Sc @ University Of Isfahan**
*2009-2014 - Electrical Engineering – Electronics*
*Design & Implementation of Networked Software Radio Receiver for Operating in VHF/UHF/L Bands*
*Under supervision of Dr Amir Reza Frouzan*
*[web]*

## Membership

**University Of Isfahan Flight Simulation Group**
*2009 to 2011 , Technical & Consultation*

**University Of Isfahan CANSAT Group**
*2011-2012 , Leader & Technical Member*

**National Institute of Elites**
*2008 – Present , Level 3 Member*

## Experience

**Various Companies**
*2004 - 2012*

**Web Developer & Programmer**

- *Design & Programming About 30 official websites for governmental organizations and corporations Including portals, online form generators ...*

**University of Isfahan**
*Physics Department*
*2011*

**Laboratory Equipment Developer**

- *Design & Construction of Contactless Laser RPM Measurement Equipment for Optic Laboratory*
- *Design & Construction of Pendulum Timing Analyzer*

**University of Isfahan**
*Radar Research Center*
*2013-2014*

**Software Radio & Signal Processing**

- *Maintain & Developing Software Radio Based Signal Processing System for Passive Radar*
- *Also Analog VHF Blocks*

**Sharif University of Technology**
*Novel Computer Architecture and Computer Network laboratory*
*2014-Now*

**DNS Service Acceleration Using GPU/FPGA**

- *Proposing an algorithm for sequential access in hash table and token verification using multiple hash functions*
- *Implementing PCI-Express 3 x8 soft core on FPGA and its linux based driver*
- *Design and implementation a cluster of beagle bone embedded boards for parallel traffic generation utilizing network boot and customized operating system*
- *Modifying 10Gb/s NIC driver for direct access to Ethernet frames*

**Sharif University of Technology**
*Intelligent information solutions*
*2015-Now*

**A Secure Digital Voice over GSM Voice Channel**

- *Design & Implementation of Soft Modem for Data Transmission over GSM Voice Channel*

**Android Operating System Customization**

- *Android Operating system customization, Building AOSP from scratch, modifying dalvik, ART and some other android stuffs*

**A Secure VOIP system from scratch**

- *Technical Manager*
- *High performance VOIP relay server* / clients written in C/C++ implementing incremental connection establishment

**ASF**
*2015-Now*

**Linux based Embedded Devices**

- *Linux customization, customize and preparing linux based operating systems from scratch for embedded and soft realtime systems*
- *Custom hardware driver development for old devices such as ISA DAQ Cards*
- *Implementing a customized operating system (based on linux) for beaglebone which boots up in just 1 second with network capability*

## Professional Qualifications

### Web Development

- Over 12 Years of Experience
- Over 35 organization portals and websites
- HTML, CSS, JavaScript (Client Side), Classic ASP (VB), PHP, ASP.net (C#)
    - My first dynamic website was a forum & portal which I wrote it with classic ASP in 2003
    - A content management system known as DLAB-SG (2005-2012)
    - Web downloader script for crawling & downloading whole website in server side
- AJAX technique
    - Implementing an ajax based windows explorer like file manager known as sonar explorer
- Adobe Flash, Action Scripting
    - Implementing e-learning system with lazy loading and content management

### Windows & Linux Development

- Over 11 Years of Experience
- C, C++, C++.net
    - Implementing a font conversation application which converts graphic images to bit patterns for using in microcontrollers
    - Implementing a digital QPSK modem for GSM voice channel
    - Implementing a high performance secure incremental connection establishment server and client with NAT traversal capability ( ~ 25000 lines of C/C++ code ) with capability of handling 100k clients
    - Implementing various hardware management applications

- Visual Basic 6
    - Implementing a coffe-net management system
    - A Trojan with lots of capabilities (something nasty)

- Worked with Microsoft MFC, QT, wxWidget and some other native platforms
    - Implementing radar UI with QT
    - Adding new features to codelite IDE (wxWidget)
    - Managing a team who develops a mobile VOIP application with QT

- Driver Development With Windows DDK
    - Studying how to implement a NDIS based network interface card driver

- Driver Development & Kernel Module Development in Linux
    - Implementing a low jitter two stage virtual timer in linux kernel
    - Developing linux drivers for Advantech ISA DAQ Cards
    - Developing linux driver for PCI-Express 3 DMA hardware implemented in FPGA
    - Modifying SMSC phy driver for faster interface wake up

- MySQL & MS Access Databases
    - Implementing a tool for converting Microsoft access databases to importable SQL code
    - Implementing a database backup & restore utility which preserves non-unicode Arabic code page entries

## Computer Graphics Development

- Over 6 Years of Experience
- Cairo graphics
  - Designed some portion of multi-function display for helicopter
  - Using Cario-GL for implementing a hardware accelerated drawing API's
- NanoVG
  - Using Nano-VG for hardware accelerated ( OpenGL ES 2.0) canvas drawing in embedded ARM system
- QML
  - Worked with QML in QT platform for drawing instruments
  - Implementing a custom native renderer under QML with Nano-VG

## Parallel Computing

- OpenMP
  - Implementing multiple hash access algorithm
  - Implementing RADAR signal processing blocks
- CUDA
  - Implementing high performance name lookup with CUDA
  - Worked with Nvidia Tesla & Titan GPU's
- Computing cluster
  - Design and implementation of compile cluster machine with help of 6, eight core machines and distcc helper
  - Design and implementation of beagle-bone cluster machine with 32 bbb boards
- Pthread
  - Extensive use of threads in ICE relay server
  - implementing a thread pool for 100k threads/connections

## Embedded Development & Digital Electronics

- AVR from 2006 , C with AVR-GCC & codeVision AVR, simulation via AVR studio & ISIS proteus
- ARM7 from 2011 , C with ARM-GCC & keil uVision
- NXP LPC series, Atmel AT91 series, STM32 series
- FPGA from 2011 , VHDL & Verilog
  - Xilinx Spartan-3, Spartan-6, Virtex-7
  - Xilinx Microblaze, EDK (XPS & SDK)
  - Modelsim simulation via advanced testbenches
  - High speed signal processing with FPGA, high bandwidth data transfer via PCI-express
  - Xilinx IP-Cores: MIG, Chip-Scope, DDS, CIC, FIR, CORDIC, FFT
  - Xilinx ISE & Vivado
- X86 based PC104 industrial computers
- Working with ARM based embedded boards like Beaglebone, Odroid, Raspberry PI, CubieBoard, Jetson Tegra K1, IMX-Rex
- Working with RT-Preempt for implementing real time tasks in linux
- Working with u-boot and barebox boot loader and their customization

### Analog Electronics , RF & Software Radio Experience

- Schematic & PCB design of mixed devices
- VHF building blocks for RADAR applications
- Software radio from 2013 , USRP , UHD & GNU Radio
- FPGA driven direct-IF all digital DSB modulation & demodulation with synchronization
- FPGA based networked software radio receiver peripheral
  ( My B.S Project ) [web]
- Data transmission over GSM voice channel ( A multi carrier QPSK modem specialized for a channel with non-linear response & high phase drift )

### Operating Systems & Embedded Related

- Linux on PC & Embedded Devices
- Linux from Scratch, Buildroot, Portage
- Kernel Modification & Customization
- Kernel Module & Driver Development
- Worked with X-Window, QT, Mesa3D, Linux Frame buffer, SDL, Cairo Graphics
- PXE-Boot Linux based operating system for computing clusters
- Android Operating System internals
  - Building AOSP from scratch for oem devices
  - Modifying android core including dalvik machine, application installer

### Aviation Related

- Flight Simulators & Their Subsystems
- Microsoft FSX & SimConnect API's
- General Avionics & Aircraft Computers

### Applications & Tools

- MATLAB & Simulink ( Communication Toolbox, Stateflow, Filter Design )
  - Implement and testing of RADAR blocks
  - Implement and testing of GSM voice mode
- ISIS Proteus & Ares, PSpice, Altium Designer
- Microsoft Visual Studio, CodeBlocks, Codelite, DevC++, QtCreator

## Research Interests & Academic Focuses

*High performance name lookup in sequential memories*
*Microcontroller Based & Embedded Designs*
*Linux Operating System*
*Networking Hardware's*
*Software Defined Radio & Communication Devices*
*Aviation & Avionic Systems*

## Awards

**2nd Rank in 10th Young Khwarizmi Festival**
*2007 – Mechanical Engineering*
*Chess Playing Robot*
*[web]*

**2nd Rank in 1st National CANSAT Competition**
*2011 – Leader , Electrical + Software's*
*University of Isfahan's Cansat Group*
*[web]*

## Publications

**Towards Using PCM/DRAM Hybrid Main Memory for Faster and Power Efficient OS Loading**
*E. Jahandar, M. Ebrahimi, M. Moradi*
*2015 – Course project report for Advanced Data Storages / Dr H. Asadi, Sharif University of Technology*
*[in English] [selected as best project and report]*

**Towards Using PID Control Approach for Dynamic Frequency Scaling in Soft Real Time Portable Media Players**
*2015 – Course project report for Embedded Systems/ Dr A. Ejlali, Sharif University of Technology*
*[in English] [selected as best project and report]*

**Design & Implementation of Software Radio Receiver Peripheral for VHF, UHF and L Band**
*2014 – My BS.c report / Under supervision of Dr A. Foruzan*
*[in Persian] [web]*

**Practical FPGA Development Video Course**
*A 5 Hour video course consist of following topics :*
*Development boards (Xilinx Spartan 3 & Spartan 6 , verilog HDL basics, design, implementation & verification tools (Xilinx ISE, Planahead, ChipScope, Modelsim, iMpact), basic & expert examples, IP-Cores (DDS, CIC, FIFO), ChipScope Based Verification.*
*2013 – [ for teaching in University of Isfahan's Digital Circuits Laboratory ]*

**Verilog HDL Self-Teach**
*2011 – Verilog Hardware Description Language Self Teach Booklet [ as reference booklet in University of Isfahan's Digital Circuits Laboratory ][web]*

## Completed Projects

### Cluster of Beagle bone black

*This is cluster computer of 32 beagle bone black embedded boards which connected to a switch. All boards have 4 GB of emmc storage and 512mb of ram with 1 Ghz ARM A7 microprocessor. A network booting facility was implemented with tftp and nfs root which hosted in raspberry pi 1 machine which runs raspbian os. The operating system of cluster nodes are custom build with buildroot and contains application needed for traffic generation especially DNS traffic. This project was part of my master thesis in Sharif university of technology.*

### Embedded Operating system + SDK/BSP for X86 PC-104

*In this project an embedded Linux operating system with full console functionality have been implemented. Developing new kernel devices drivers, high precision timer in kernel space, modifying boot loader for faster boot process, custom made file system utilities and init system, customized build of compilers/toolchains and preparing SDK for this operating system, integrating and modifying an open source IDE for adding host-target / host-emulator capabilities to the SDK, preparing emulator for the operating system and some other are done in this project. The operating system boots up in less than 1 second in 800Mhz Vortex-X86 CPU with 128Mb of flash disk.*

### Data Modem over GSM Voice channel

*This is Data modem which transmits digital data over voice channel of GSM network. This modem is a part of end to end crypto phone. This modem receives digital data from one side and modulates the data with multicarrier QPSK modulation. The modulated signal fed to GSM voice channel via GSM module and the receiver performs the demodulation and extracts the original transmitted data. Digital communication over GSM voice channel is challenging. The GSM voice channel has a nonlinear phase, low SNR & Dynamic range. Also there's voice activity detector in GSM handsets which makes the work harder. At first modem was implemented in MATLAB Code and then implemented with pure C under Linux and tested with embedded devices such as raspberry pi and odroid. The Modem could achieve bitrate of 1.4kbps with BER near zero.*

### 120Gbps FPGA Based Layer II firewall

*This is the layer 2 network firewall completely implemented on FPGA Board. It has 12 SFP+ Optical cage connected directly to Virtex 7 690T FPGA. This firewall can process 127 Million packet per second and achieving 60 Gbps bidirectional network throughput and 120 Gbps in unidirectional and programmed with a basic set of commands from another external port. This firewall is a complete solution for backbone ISP's, datacenters and revealed in second national domestic made cyber equipment's exhibition.*

### ESDR a Software Radio Receiver Peripheral

*Software Defined Radio is a new communication technology which implements nearly all of the processing blocks in digital domain. Every software radio system has receiver system. in this project I have built a software radio receiver peripheral named ESDR, this receiver has an VHF/UHF/L-Band analogue tuner, 40Msps 10Bit A2D, two FPGA's, network interface and GNU Radio source driver. The receiver capable of receiving signals from 50Mhz to 2.2Ghz with an I-Q representation and sample rates up to 2.8Msps for single I-Q channel and 1.4Msps for dual I-Q channels. it has an internal Digital Down Convertor and network interface to communicate with PC based GNU Radio Digital Signal Processing software.*
*2014. Thesis Report & More Information's Available on My Website .*

### Passive Radar Software Radio Signal Processor

*The passive radar needs sophisticated signal processing for extracting very weak echoed signals with small amount of Doppler shift from high power interference. The software processor was written in C++ in GNU-Radio environment as out of tree module. The software processor incorporates an adaptive LMS filter, 2-D match filter and 2-D CFAR processor and display subsystem in one application. Drawings are done in QT and some adaptive filter processing are done in GPU for faster frame generation.*
*2014 – [ I wasn't original & first author of the processor]*

### All Digital FPGA Driven DSB Modulation & Demodulation

*The project consists of two sections which developed independently on two FPGA evaluation boards. First one is modulator which receives sound from music source and produce DSB modulated signal at IF Band. The second board samples the IF signal with onboard 40Msps A2D. DSB Demodulations done in FPGA with assist of synchronization section and finally produces extracted sounds from IF signal.*
*2012*

### Aircraft Autopilot Test bench using Microsoft Flight Simulator

*An application written in C++ under Microsoft Native VC++ which connects to Microsoft Flight Simulator using standard API's and provides aircraft flying parameters to autopilot controller. The connection provides capability to send & receive commands from Flight Simulator which could be used for autopilot Test bench for testing the autopilot behavior in pseudo real world with visual inspections. The autopilot consist a simplified control system for Bank & Pitch control of aircraft and manage the aircraft to reach specific point at desired speed & altitude.*
*2012*

### CAN SAT

*The Cansat is Can Shaped Mini Satellite which is Simulating a Real Micro Satellite's Life Cycles and Workarounds, the Cansat Uses an Low Power ARM7TDMI Microcontroller to Collect Data From Sensors , Analyses them, Saving them and Sending Back to Ground station.*
*2011 Reports & More Information's Available on My Website .*

### Embedded Graphic Rendering System

*In This Project I built a Customized Linux Kernel and Other Stuffs to Make A Fast & Reliable Embedded Linux Core. The Work Proceeded Under an X86 PC-104 Compatible Mini Computer with CF Memory Storage and Some Sorts of IO. The Computer Has Intel 1.4Ghz X86 Processor & 256Mb of Ram. The Developed Embedded Operating System Loads in Only 0.6 Second (From Boot loader to Bash). Also I Implemented A Native frame buffer device driver based on Cairo Graphics Rendering Suite.*
*2010 – The Boards & Stuffs Was Offered by Iran Aircraft Manufacturing Company.*

### Contactless Laser RPM Meter

*A RPM Meter Which Measures the Revolution Per Minute ( And Second ) with Laser Beam and Reflected Beam Pulses.*
*2010 - Optic Laboratory of University of Isfahan*

### Ultra Sonic Air Thermometer

*A Thermometer which measure the Speed of Sound in Air And Calculates the Temperature from the Sound Speed & Humidity of Air.*
*2008*

### Chess Playing Robot

*This is a Standalone Robot that can Play Chess With a person Physically. This robot utilizes a Magnet Sensitive Chess board which recognizes piece movements, the MCU Core of the robot Calculates the Moves and Send Command's to Motors to Make a Move.*
*2006 – 2007 [web]*

### Persian / Arabic Graphic LCD Text Rendering API's

*This is an API Library which is used for Native Persian Text Rendering in GLCD's. The Library made Open Source and Published in [web]*
*2007*

### Prayer Times Clock

*This is special Clock which designed for Muslim Peoples to Automatically Play Adhan in Prayer Times. The User Just Specify the Date Time & City in Clock Settings and the Clock Calculates the Prayer Times and Play Adhan in Those Times Automatically. The Clock Uses and Low Power AVR Microcontroller and Graphic LCD for Displaying Times and …*
*2007*

### Sonar Explorer

*A Web based AJAX File manager which has similar Web Interface Like Windows XP Explorer. The system was developed with PHP, extensive javascript and CSS. [web]*
*2005*

### Web Downloader

*Web Downloader is a Web Based Application Which can Download A Website Completely With Server's High Speed Internet Connection And Zip them, Then Sends the Zipped File To User. This Application Has Various Algorithms and Methods to Collect Web Links and Download Them.*
*2005*

### DLAB-SG

*DLAB site generator (DLAB-SG) was a complete portal system which I developed and used it between 2003 and 2012 in about 30 official governmental websites. One university, 3 major regional news website's, two municipalities, two governments, 12 state companies and over 20 other websites used DLAB-SG as their portal system. The portal was powered by PHP+MySQL database and as today no security vulnerabilities are reported [in sites more than 10000 visitor per day].*
*2005-2012*

### Coffenet Station Accounting / Controlling system

*This was my first commercial project. It was complete server/client system which could be used for controlling and generating usage invoices for coffenet internet stations. The program written in Visual Basic 6 with help of Access database. Server application had a graphical UI + an small web based controlling interface. Web interface was developed with classic ASP.*
*2003*

## Current Working Projects

### Secure High Performance VOIP System

*This is secure VOIP system which completely designed by our team. We don't use any existing standards for our security and performance concerns. The implemented VOIP server has ability of implementing ICE like protocol for offloading VOIP traffics from our relay server and makes peer-peer connection even if both peers are behind of NATed networks. The server written in pure C and we used OpenSSL just for cryptographic operations. This system has all major features of modern VOIP system such as authentication, key-exchange, QoS, and …*

### BSTN Communicational Protocol & Physical Layer

*BSTN Stand's for BUS Switched Telephone Network. BSTN is Telephony Network which uses Bus Network in High speed for Nodes Communications and Targeted For Large Out-of-Tree Telephony Networks in Organizations. BSTN Has Several Interfaces with Some Other Types of Telephony Networks such as VoIP & PSTN for its Compatibility.*
*This Project is Under Fund of University of Isfahan , Vice Chancellor of Research .*

### Hardware Accelerator for DNS Server

*This is my MS.c project at sharif university of technology. The Project consist of FPGA board and custom linux driver and modified version of DNS server software. The board is a Virtex7 FPGA board with Gen3 PCI-Express, 12 10GBit SFP+ Ports, DDR3 and QDR memories. The board along with its programmed FPGA receives DNS traffic with its 10Gbe ports. Processing DNS traffic will be done in FPGA with help of host PC and its software's. This project aims to improve query per second in DNS servers from a few thousands to hundreds of thousands which is a big improvements in DNS servers.*